

FIG. 100 is a block diagram of a system architecture, enclosed in a dashed box labeled 100. The system is divided into two main sections, 110 and 120, which are connected to a central M INT block. Section 110 (left) includes a JTAG block (131) connected to a DSP CORE (11) and PERI (15). It also contains SARAM (14), DARAM (13), and ROM (12). A bus M1 connects these components to the M INT block. Section 120 (right) includes a DSP CORE (21) and PERI (25). It also contains SARAM (24), DARAM (23), and ROM (22). A bus M2 connects these components to the M INT block. Both sections have external I/O (EXT I/O) and are connected to a common X ARB (136) and XC2 block. The M INT block is connected to two M ARB blocks (17 and 27), which in turn connect to DMA and HPI blocks (18 and 28). The system is also connected to a common XC2 block (29) and a common X ARB (136) and XC2 block (138). The system is connected to a common X ARB (136) and XC2 block (138) and a common X ARB (136) and XC2 block (138).

FIG. 2

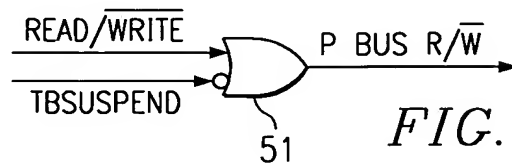
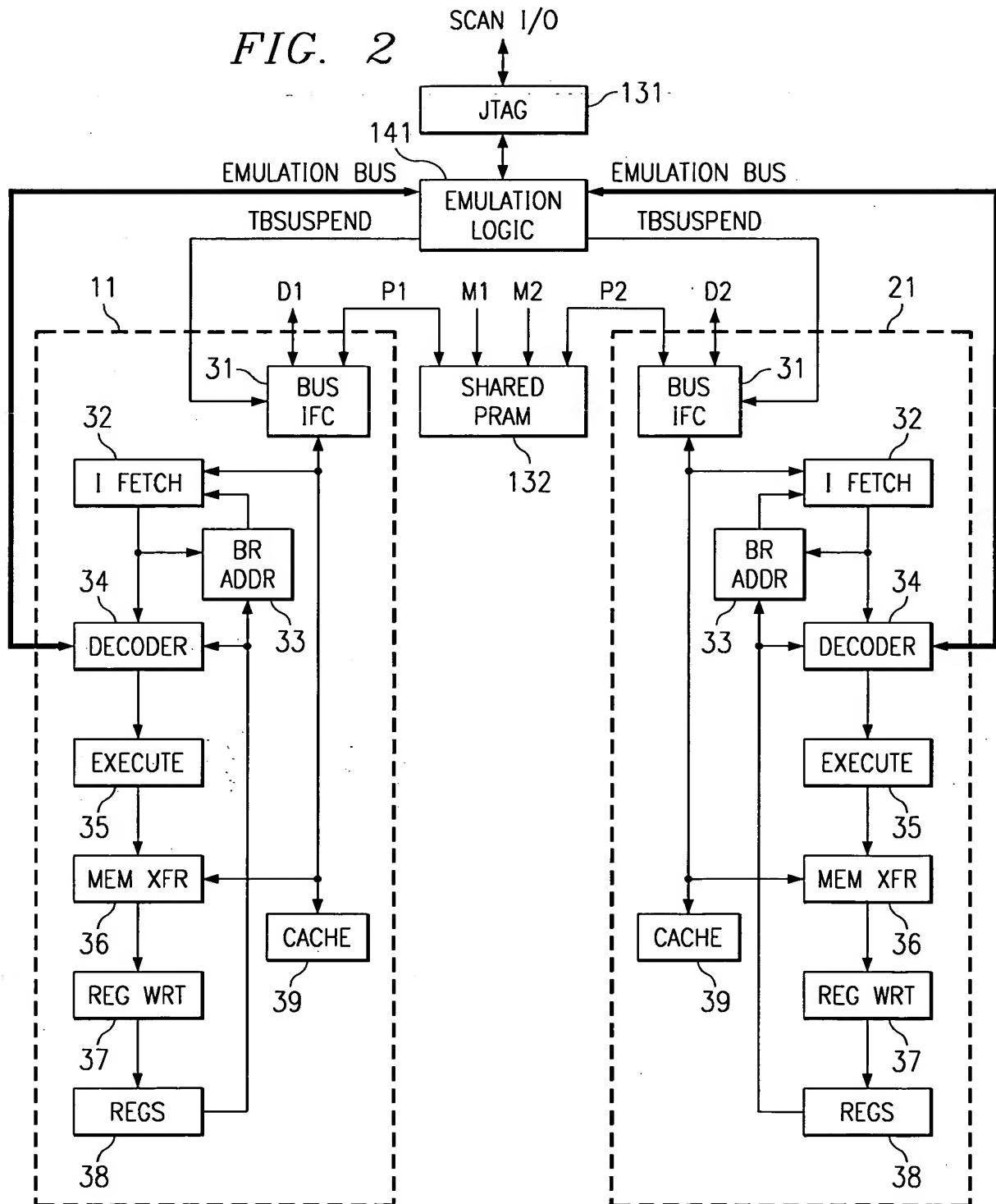


FIG. 3